hansenanotec

HansePhotonik

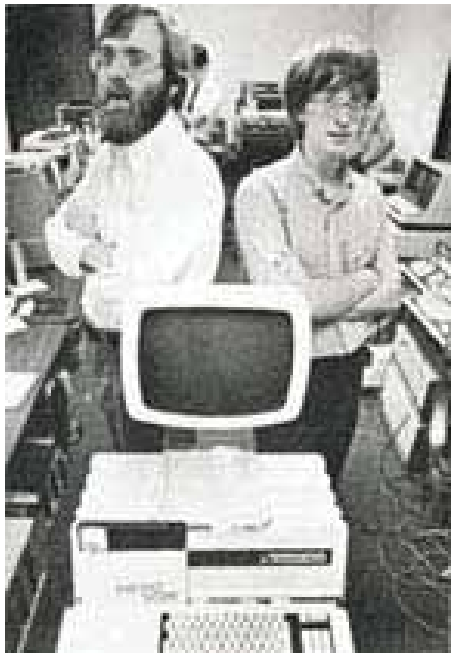
Unternehmensgründung im Hightech-Bereich:

Eine alternative Karriere

Dr. Michael Lübbehusen,
geschäftsführender Gesellschafter

MAZ level one

Vom Gründer zum reichsten Mann der Welt:



Aller Anfang ist schwer...

- **Die Technologie ist innovativ, aber...**
  - ...ist nicht oder nur unzureichend geschützt.
  - ...ist technisch kompliziert und unverständlich.
  - ...hat ihre Machbarkeit noch nicht bewiesen.
  - ...besitzt ein noch unklares Marktpotential.
  - ...benötigt eine risikoreiche Startinvestition.

"Want to be his second customer?"

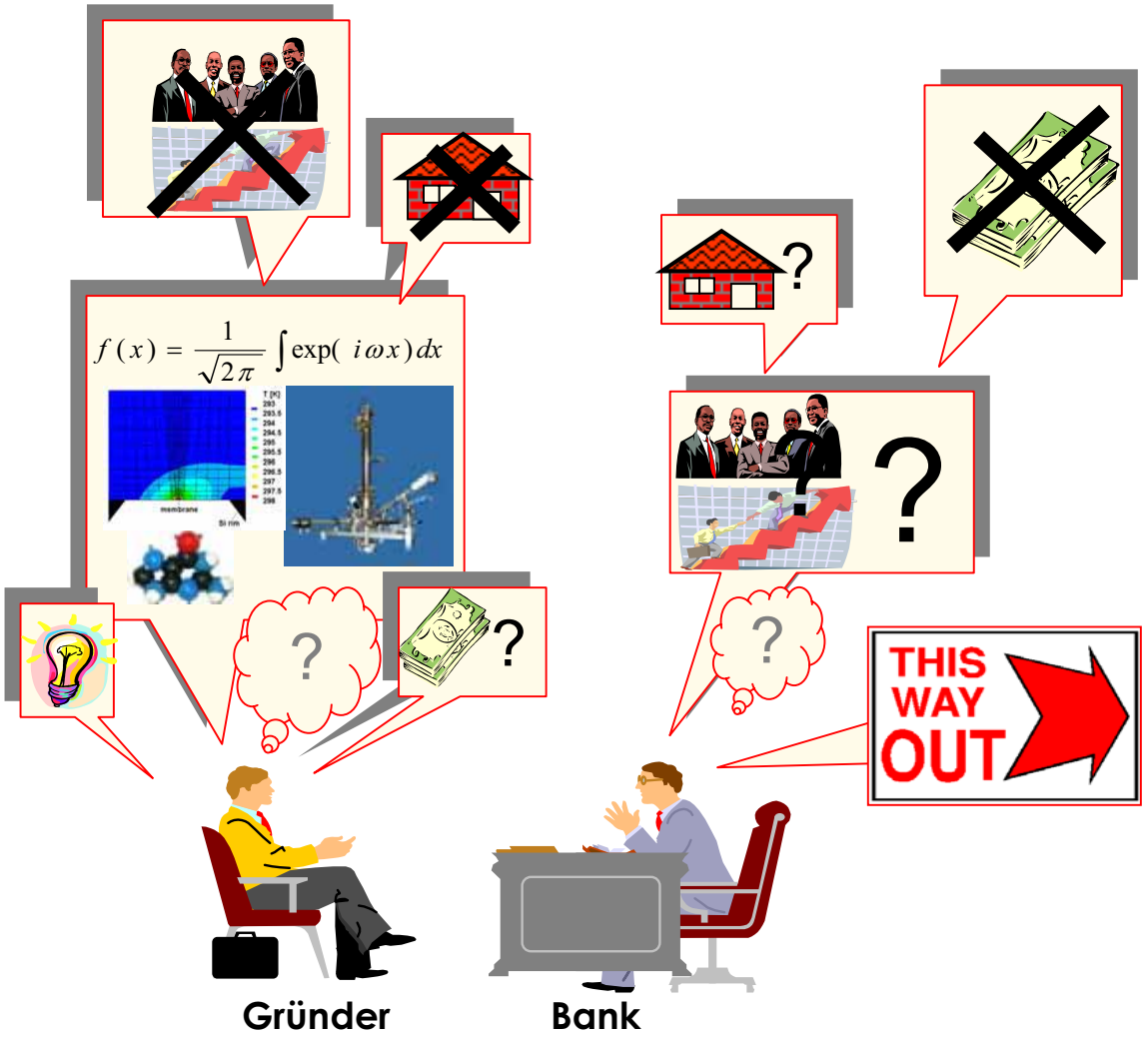
- **Die Gründer sind hoch motiviert und talentiert, aber...**
  - ...verfügen über kein spezifisches Branchen Know-how.
  - ...besitzen keine kaufmännischen Grundkenntnisse.
  - ...wissen nicht, wie Beteiligungskapital funktioniert.

- **Eine Kapitalgesellschaft ist noch nicht gegründet...**
  - ...und hat noch kein Beteiligungskapital akquiriert.

Unternehmensgründung: Wo gibt´s Geld?

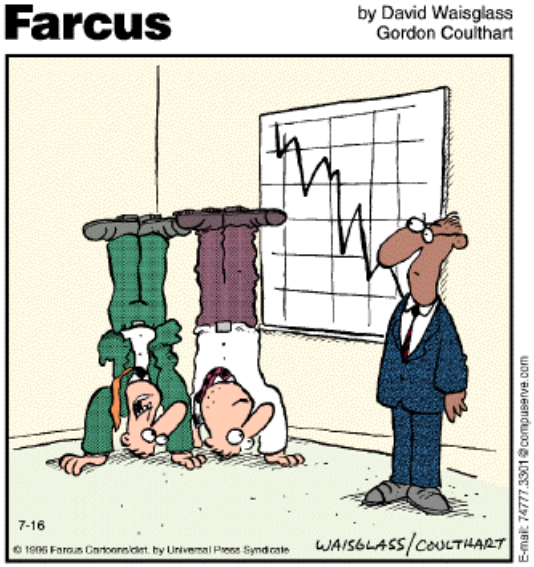
- **FFF**: **F**ools, **F**amily, **F**riends
- **Arbeitsamt**: Gründung aus der Arbeitslosigkeit
- **Öffentliche Förderung**: bis zu 50% bei entsprechendem Kapitalnachweis, hoher bürokratischer Aufwand; Ausnahme: Ideen FONDS bis zu 50 T€ (www.c-bs.de)
- **Banken:** Kredite nur gegen Sicherheiten, Zinsen belasten das laufende Geschäft, Gründer muss persönlich haften
- **Öffentliche Banken (KfW)**, **Beteiligungsgesellschaften**: Nur Kofinanzierungen mit einem Leadinvestor, KfW mit Sonder-programmen für Gründer (ww.kfw.de, www.tbg-bonn.de)
- **Venture Capital oder Risikokapital, Businessangel** (www.bvk-eV.de, www.bachh.de)

Technology meets Finance



Ideen brauchen Struktur – Die Businessplanung

- Roter Faden der Geschäftsentwicklung
- Basis für die Investitionsentscheidung
- Erfolg wird messbar (Meilensteine)
- Ist niemals fertig
- Typischer Inhalt:
  - Executive Summary (Zusammenfassung)
  - Management Team (Qualifikation und CV)
  - Businessmodel
  - Produkt / Alleinstellungsmerkmale (USP´s) / Kundennutzen
  - Branche / Markt / Wettbewerb
  - Marketing und Vertriebsstrategie
  - Finanzteil: 3 - 5 Jahres Vorschau auf Umsatz, Investitionen, Personal, cash-flow, Finanzbedarf..., GuV, Bilanz, ...



"It depends on how you look at it, sir."

Start mit MAZ level one

- Finanzierung und Betreuung sehr junger, wachstumsstarker Technologieunternehmen bis zu 500.000 € pro Beteiligung
- Vollständige kaufmännische Unterstützung (toolbox)
  - Alle Gründungsprozesse
  - Jahresabschlüsse
  - Reporting / Controlling / Organisation der Buchhaltung
  - Förderanträge
  - Personal
- Geschäftsmodell und Businessplanung
- Vertriebs- und Markteintrittsstrategien
- Ergänzung des Managementteams
- Vollständige Erstellung der Due Diligence Unterlagen
- Nächste Finanzierungsrunde

B Wieso können wir das?

- GFs sind selber Gründer und Einwerber von Beteiligungskapital
- 15 High-Tech Unternehmensgründungen
- über 25 Mannjahre Erfahrung im Seed-Bereich
- 8 erfolgreiche Verkäufe unserer Beteiligungen bei aktiver Gestaltung des Verkaufsprozesses
- Mehr als 15 Jahre Geschäftsführungserfahrung in zahlreichen Technologie-Start-Up´s
- Keine Insolvenz in der Seed-Phase
- Kaufmännische und technologische Kompetenz
- Gute und hilfreiche Kontakte

B Wachstumsstarke Technologieunternehmen ?

- Branchenerfahrenes Top Management Team
- Durchhaltevermögen, höchste Motivation und Einsatzbereitschaft
- Reich werden wollen
- Eigene finanzielle Beteiligung
- Erfolg teilen können
- Teamgeist
- Technologie mit schützbaren Alleinstellungsmerkmalen
- Gute Exit-Möglichkeit
- Wachstumsmarkt mit 100 Mio €
- Finanzbedarf passt zum Unternehmenswert

Beispiel:

Weltweit kleinster Gaschromatograph in Mikrosystemtechnik:

- Sehr schnelle Analyse
- Faktor 100 weniger Energieverbrauch
- Faktor 1000 weniger Analysevolumen
- Mobiler Einsatz eröffnet völlig neue Anwendungen
- www.slsmt.de

Stefan Exner
CEO
Dipl.-Wirtschafts-Ing.

Uwe Lehmann
CTO
Dipl.- Phys.
TUHH 2001

Beispiel:

Feed-Forward Approach for Automatic PMD-Compensation at 80 Gbit/s over 45 km Installed Single Mode Fiber

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Abstract: We report 80 Gbit/s transmission over 45 km installed fiber employing automatic PMD-compensation. A feed-forward controller adjusted the DGD of the PMD compensator in a single step avoiding the need for dithering.

Introduction

Polarization mode dispersion (PMD) causes severe signal impairments in high bit-rate optical transmission systems. Since there is still no established method for compensating PMD, telecommunication companies cope with this problem by using selected low-PMD fibers and reducing the transmission distance. In OTDM systems with bit-rates significantly higher than 40 Gbit/s, PMD limitations cannot be overcome by this approach since PMD reduces the signal quality even with low-PMD fibers.

A critical issue in every adaptive control system is its response time. Previous investigations have shown that a response time in the millisecond range is desirable for PMD-compensation [1]. If the parameters of the equalizing unit have to be dithered to find the optimum settings, this implies that the response time of the equalizing elements has to be shorter by an order of magnitude.

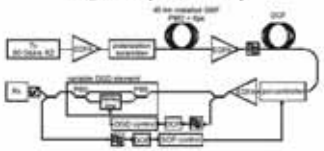
We reduce this requirement for the differential group delay (DGD) element of the compensator by applying feed-forward control in an open loop. In our experiment, the link DGD is continuously measured and fed forward to a variable DGD element in order to set the appropriate DGD of the compensator in a single step. Continuous DGD monitoring is realized by a polarization-resolved evaluation of the degree of polarization (DOP) combined with a polarization scrambler at the fiber input [2]. In this way the DGD of the link can be monitored at any time and the dependence on the input polarization is eliminated.

Using this PMD compensator, we performed the first error-free transmission of an 80 Gbit/s RZ data signal over a PMD-compensated installed fiber link of 45 km length with an average DGD of 6 ps.

DGD Measurement

In presence of PMD the DOP of the received signal is reduced. The amount of reduction depends not only on the DGD but also on the power-splitting ratio γ of the two principal states of polarization (PSP). The reduction is maximum for γ=0.5. Recent concepts propose to use the DOP as a quality signal in a feedback control loop [3,4]. Since the reduction of the DOP depends on the power-splitting ratio γ, it is not possible to derive the link DGD from the measured DOP alone. Thus these concepts maximize the DOP by dithering all parameters of the equalizing unit.

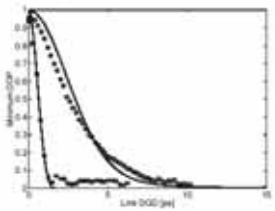
Figure 1: Experimental Setup



However, it is desirable to measure the DGD and the PSP of the fiber directly so that an equalizing unit can move directly to the appropriate state in a single step avoiding the need for dithering.

We applied this concept to the DGD control of our PMD compensator by using a polarization scrambler at the fiber input and by monitoring the DOP and the state of polarization (SOP) at the fiber output [2]. Since the scrambler causes the input polarization to cover the whole Poincaré-sphere within 18 ms, the minimum DOP occurring within that time interval belongs to a power-splitting ratio of 0.5 and allows to derive the link DGD. The PSPs can be determined by monitoring the SOP with the largest DOP within that time interval. [2,5].

Figure 2: Measured DOP response curve (squares: without bandpass filter, circles: with 1.2 nm bandpass filter), solid lines: simulation results.



- 40 Gbit Datenübertragung
- Entwickelt an der TUHH
- gegründet in 2001
- www.adaptif.de

Ralf Stolte
CEO
Dr.-Ing.
TUHH 1994

Harald Rosenfeldt
CTO
Dr.-Ing.
TUHH 2002

Beispiel:

Mapping Instruction Sequences onto EPOM-Processor Arrays :
A Framework for Parallel Data Processing

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Abstract

This paper introduces an optimized mapping methodology for mapping instruction sequences (ISs) onto EPOM-processor arrays. The new features of this mapping methodology result from a systematic specification and exploitation of both instruction and processor level parallelism : ultra-low granularity of ISs requires an allocation and scheduling of individual instructions onto the given processor array. Moreover, this mapping methodology is complete in the sense that it considers both array bus-bandwidths and processor resource constraints. The mapping methodology is based on two concepts. 1. instruction sequences (ISs): they represent a generalized form of directed cyclic graphs (DCG's) and allow to efficiently specify algorithm parallelism. Graph nodes represent instructions out of the instruction set of a target processor architecture [The96a] [The97a] 2. the EPOM-processor architecture : it represents an optimized target VLIW-processor architecture (in terms of cost and performance) for parallel implementation of ISs [The96a] and especially suited for parallel image/multimedia processing [The95]. In this paper, special attention is paid to the optimization of the mapping process of ISs onto EPOM-processor arrays. Algorithm execution time minimization is used as optimization goal. The mapping methodology is partially based on integer-linear-programming and heuristic techniques. The solution time complexity is substantially reduced by developing a two-phase hierarchical model, decoupling processor-array allocation from subsequent scheduling. The efficiency of this mapping methodology has been validated through experimental results on ISs of well-known algorithm routines.

Keywords— **instruction sequence, instruction / processor level parallelism, mapping methodology, EPOM-processor arrays, minimal execution time, resource constraints**

0 Preliminary Remarks

This paper is not self-contained. It often refers to the concepts and properties of EPOM-processor arrays. Therefore, the interested reader is referred to [The95] [The96a] [The97a] for a complete discussion of POM and EPOM-processor architectures. However, although this knowledge may help the reader to get familiarized more quickly with the concepts presented in this paper, it is not necessary for a full understanding. The aim is simply to avoid overlength of the paper as well as to keep the burden of concepts and definitions to a strict minimum.

1 State-of-the-art mapping methodologies

In this section, we briefly discuss existing software synthesis and compilers techniques for mapping algorithm and task graphs onto processor systems. We point out their limitations and use this short overview study as a motivation to develop our mapping methodology which aims at overcoming some of the major limitations of existing methodologies.

We classify existing mapping methodologies into three major groups according to the scheduling techniques, the algorithm class, the target architectures and the resource constraints that are considered.

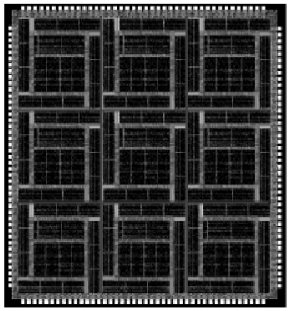


Fig. 1a : 3X 3 EPOM-processor array built up with (2,4,4,P)-EPOM-processors

AnteVista
microprocessor technology

- Mikroprozessor-Architektur
  - 3-7 x schneller
  - 2-5 x weniger Power
- gegründet in 2001
- www.antevista.de

Jean-Paul Theis
CEO
Dr.-Ing.
ETH Zürich 1996

MAZ level one

Beispiel: INCHRON advanced design automation



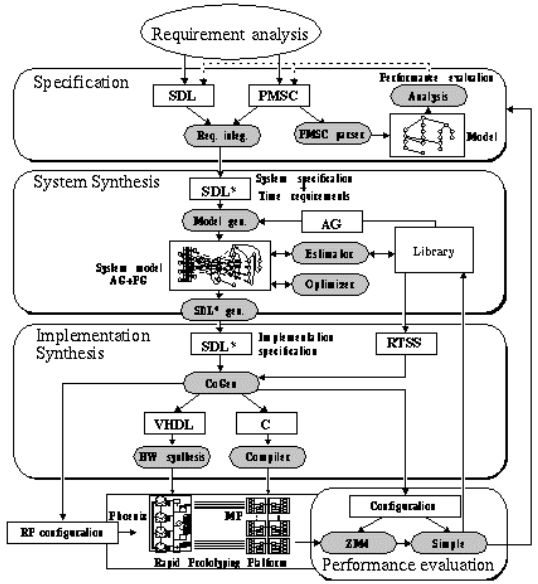
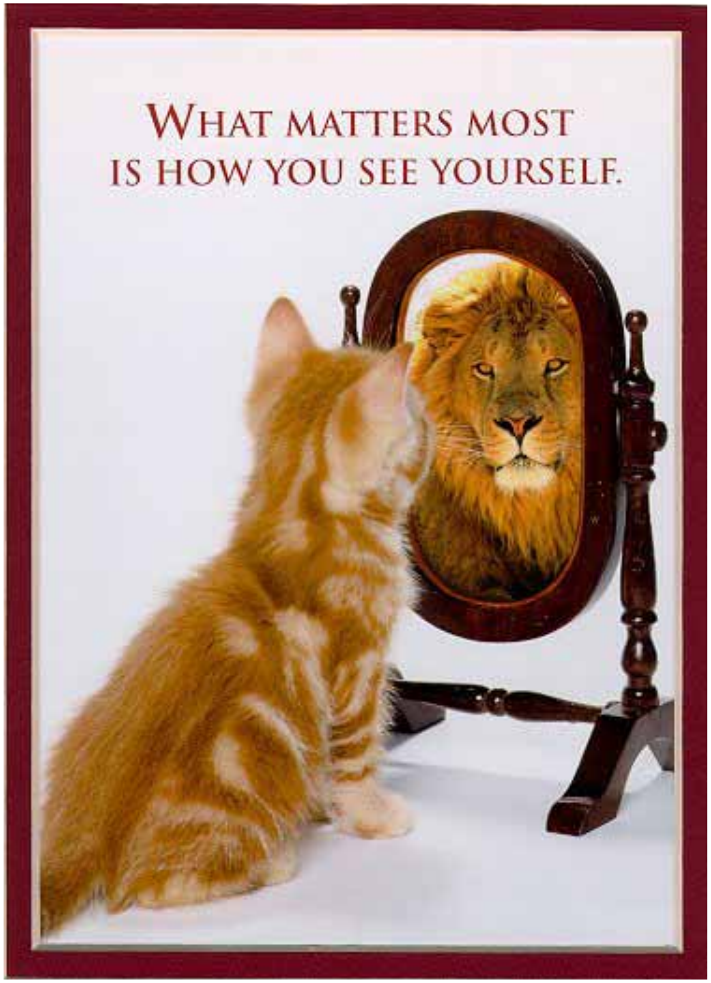



Figure 1: Design flow

Entwurf und Simulation eingebetteter Echtzeitsysteme

- Wissenschaftliche Mitarbeiter am Fachbereich Informatik, Universität Erlangen
- 2001 Hochschulgründerpreis und Preisträger Businessplan-wettbewerb Nordbayern
- 2002 Start-up Wettbewerb
- 2003 Gründung der GmbH mit MAZ level one
- www.inchron.com

MAZ level one



Danke für Ihre Aufmerksamkeit!

www.mazlevelone.com